Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A successive approximation analog-to-digital converter comprising:

an analog sample and hold circuit;

a switched capacitor DAC having an input coupled to an output of the sample and hold circuit;

a comparator having an input coupled to an output of the switched capacitor DAC;

a plurality of set-reset latches, each set-reset latch being responsive to a combination of control signals and the output of the comparator and configured to provide ~~non-overlapping~~first and second switch driver signals having first and second states as set-reset latch outputs, the first switch driver signal being in the first state when the set-reset latch is set, the second switch driver signal being in the first state when the set-reset latch in reset, the first and second switch driver signals not being in the first state at the same time;

the switch driver signals being coupled to control the switched capacitor DAC.

2. (Currently Amended) The converter of claim 1 wherein the switched capacitor DAC is a differential switched capacitor DAC, the set-reset latches each also providing third and fourth switch signals, the third switch driver signal being in the first second when the set-reset latch in set, the fourth switch driver signal being in the second state when the set-reset latch in reset, the third and forth switch driver signals not being in the second state at the same time .

3. (Original) The converter of claim 1 further comprised of a controller coupled to provide the control signals.

4. (Original) The converter of claim 3 wherein the controller is a state machine.

5. (Original) The converter of claim 1 wherein the set-reset latches have switch driver signal outputs that are level shifted in comparison to the combination of control signals and the output of the comparator.

6. (Original) The converter of claim 1 wherein the set-reset latches are NOR gate based latches.

7. (Original) The converter of claim 1 wherein the set-reset latches are NAND gate based latches.

8. (Canceled)

9. (Original) The converter of claim 1 wherein the switched capacitor DAC is a binary coded DAC.

10. (Original) The converter of claim 1 wherein the switched capacitor DAC is a reduced radix DAC.

11. (Original) The converter of claim 1 wherein the switched capacitor DAC is a mixed radix DAC.

12. (Currently Amended) A successive approximation analog-to-digital converter comprising:

an analog sample and hold circuit;

a differential switched capacitor DAC having an input coupled to an output of the sample and hold circuit;

a comparator having an input coupled to an output of the switched capacitor DAC;

a plurality of set-reset latches, each set-reset latch being responsive to a combination of control signals and the output of the comparator and configured to provide ~~non-overlapping~~ first, second, third and fourth switch driver signals as set-reset latch outputs, each switch driver signal having first and second states as set-reset latch outputs, the first switch driver signal being in the

first state when the set-reset latch in set, the second switch driver signal being in the first state when the set-reset latch in reset, the first and second switch driver signals not being in the first state at the same time, the third switch driver signal being in the second state when the set-reset latch in set, the fourth switch driver signal being in the second state when the set-reset latch is reset, the third and forth switch driver signals not being in the second state at the same time; and,

a controller coupled to provide the control signals;

the switch driver signals being coupled to control the switched capacitor DAC.

13. (Original) The converter of claim 12 wherein the set-reset latches have latch outputs that are level shifted in comparison to the combination of control signals and the output of the comparator.

14. (Original) The converter of claim 12 wherein the set-reset latches are NOR gate based latches.

15. (Original) The converter of claim 12 wherein the set-reset latches are NAND gate based latches.

16. (Canceled)

17. (Original) The converter of claim 12 wherein the switched capacitor DAC is a binary coded DAC.

18. (Original) The converter of claim 12 wherein the switched capacitor DAC is a reduced radix DAC.

19. (Original) The converter of claim 12 wherein the switched capacitor DAC is a mixed radix DAC.

20. (Currently Amended) In a successive approximation analog-to-digital converter, the improvement comprising:

a plurality of combined set-reset latches and switch drivers responsive to a combination of control signals and the output of a comparator to provide successive approximation switch signals to a switched capacitor DAC, each combined set-reset latch and switch driver having a set-reset latch having ~~non-overlapping~~ first and second switch driver signals as latch outputs, the first switch driver signal being in the first state when the set-reset latch is set, the second switch driver signal being in the first state when the set-reset latch in reset, the first and second switch driver signals not being in the first state at the same time.

21. (Original) The improvement of claim 20 wherein the set-reset latches having switch driver signals as latch outputs have latch outputs that are level shifted in comparison to the inputs to the set-reset latches.

22. (Currently Amended) A method of providing latched ~~non-overlapping~~ switch driver signals comprising:

providing a set-reset latch responsive to latch control signals referenced to a first voltage and having ~~non-overlapping~~first and second latch output signals, the first latch output signal being in the first state when the set-reset latch in set, the second latch output signal being in the first state when the set-reset latch in reset, the first and second latch output signals not being in the first state at the same time;

powering the latch at a second voltage different than the first voltage;

coupling the ~~non-overlapping~~ latch output signals as ~~non-overlapping~~ switch driver signal outputs.

23. (Original) The method of claim 22 wherein the second voltage is higher than the first voltage.

24. (Currently Amended) The method of claim 22 wherein the first state is a high logic state~~non-overlapping signals are non-overlapping in the positive logic sense~~.

25. (Currently Amended) The method of claim 22 wherein the first state is a low logic state.~~non-overlapping signals are non-overlapping in the negative logic sense.~~

26. (Currently Amended) The method of claim 22 wherein the set-reset latch also has third and fourth latch output signals, the third latch output signal being in the second state when the set-reset latch in set, the fourth latch output signal being in the second state when the set-reset latch in reset, the third and forth latch output signals not being in the second state at the same time ~~the non-overlapping signals comprise two non-overlapping signals in the positive logic sense and two non-overlapping signals in the negative logic sense~~.